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| **Citation** | Niels Van Thienen, Patrick Reynaert, 2014,<br>**Title**<br>Electronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on, p104-107. |
| **Archived version** | Author manuscript: the content is identical to the content of the published paper, but without the final typesetting by the publisher |
| **Published version** | http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7049942 |
| **Journal homepage** | |
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# A 160-GHz Three-Stage Fully-Differential Amplifier in 40-nm CMOS

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***Abstract* — This paper presents a 160-GHz fully-differential power amplifier in 40-nm CMOS. A tapered gate-connection network was optimized which results in a reduction of the gate resistance and allows to achieve a maximum gain of 11.6 dB with a 3-dB bandwidth of 24 GHz from the three-stage amplifier. The measured saturated output power is 4.1 dBm and the measured 1-dB compression power is 1.5 dBm. The matching networks are implemented using on-chip transformers and slow-wave transmission lines. Differential and common-mode stability is obtained by adding cross-coupled capacitance to the differential pairs and series resistance to the bias network respectively. The amplifier core occupies an area of 0.063 mm$^2$ due to the compact design and the use of slow-wave transmission lines. With a supply voltage of 1.0 V, the amplifier consumes a DC current of 42 mA.**

***Keywords* — CMOS, Fully-differential, G-band, mm-Wave, Power amplifier, Transformer-coupled.**

## I. Introduction

Nowadays, when smaller technologies are available, integrated circuits in the 140-220 GHz (G-band) frequency range are realizable in standard CMOS. High-performance power amplifiers gain in importance due to the rising trend of new high-frequent applications, such as mm-wave medical imaging, automotive radar and wide-band communication systems. All these systems benefit from the high bandwidth that is available at mm-wave frequencies. Therefore, high-performance amplifiers with sufficient power gain and bandwidth are required.

The aim of this paper is to design a power amplifier with maximum power gain at an operating frequency of 160 GHz. Differential and common-mode stability are especially emphasized during the design process. Several techniques to improve the high-frequent performance were successfully implemented and will be discussed in Section II. In Section III, the measurements confirm the correctness of the performed simulations and the proposed design techniques. Conclusions are given in Section IV.

## II. Circuit Implementation and Optimization

Every stage of the three-stage amplifier consists of a cross-coupled neutralized pair. This basic amplifier stage is illustrated in Fig. 1. It is important to maximize the gain per stage. This results in a lower DC power consumption and a higher 3-dB bandwidth for the same overall gain. This is done by (1) reducing the gate resistance $R_g$, (2) adding cross-coupled capacitors $C_N$ to the differential pair and (3) using an optimized tapered connection network to connect the gate and drain of the NMOS transistors with the top-metal transformers. The aforementioned techniques allow to minimize the number of stages.

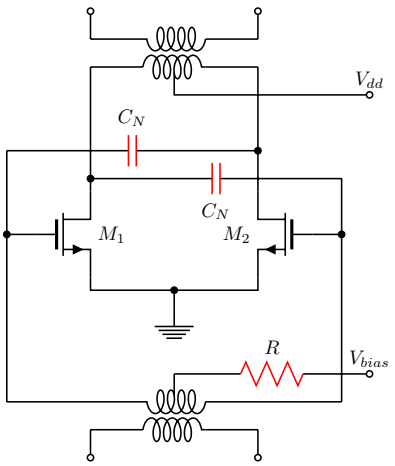
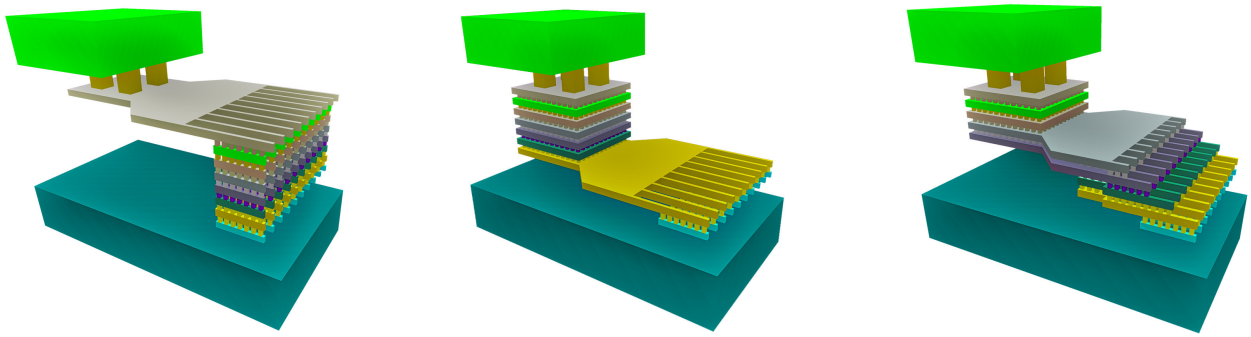



Fig. 1. Schematic of one single stage of the amplifier with a cross-coupled neutralized NMOS differential pair and a resistive bias network.

### A. Tapered Connection Network

Fig. 2 shows the layout of the tapered interconnect between the top-metal transformer (metal 9 and 10) and the drain of the transistor (metal 1). To connect the gate of the transistors, a similar structure is used. As such, both drain and gate structures are interleaved. The interconnect has to bridge a vast gap over 10 metal layers, which will reduce the gain. Three different implementations - a straight up, a flat and a tapered structure - have been investigated. The straight up, rigid connection (Fig. 2a) has a low resistance, but it has an increased capacitance between the gate and drain fingers. The flat structure (Fig. 2b) minimizes the capacitance between these fingers, but creates a high capacitive coupling to the substrate. This imposes a trade-off between resistance and capacitance. In order to optimize each amplifier stage in terms of gain,



(a) (b) (c)

Fig. 2. Implementations of the metal stack to connect the NMOS transistor (metal 1) with the top-metal transformer (metal 9-10): (a) straight up structure, (b) flat structure and (c) tapered connection network with minimum parasitics.

the tapered structure (Fig. 2c) was designed for minimum parasitic capacitance and resistance. Fig. 3 illustrates the gain improvement of the tapered connection network simulated in ADS Momentum. At 160 GHz, more than 1 dB additional gain is achieved per stage, this results in 3 dB gain for the entire amplifier.

### B. Active Devices

Both gain and stability are further improved by adding cross-coupled capacitors [1] and splitting the transistors into multiple fingers. A multi-finger layout is necessary to optimize the transistor performance at frequencies close to $f_{max}$ in terms of gain and stability. Furthermore, the reduced finger width ($W_f$) produces a lower gate resistance $R_g$. A well-designed transistor can achieve a higher $f_{max}$ as such, resulting in a higher power gain. The gates of transistors $M_1$ and $M_2$ are split into 20 fingers, each with a minimum length ($L$) of 40 nm and a finger width of 1 µm, which leads to a total width ($W_{total}$) of 20 µm. The cross-coupled capacitors $C_N$ are implemented by MOMcaps. For

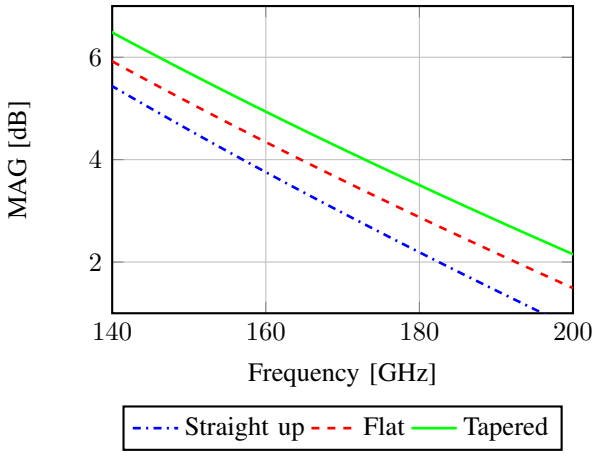



Fig. 3. Simulated maximum available gain (MAG) for a differential pair ($L$ = 40 nm, $W_f$ = 1 µm, $W_{total}$ = 20 µm and $C_N$ = 6 fF) with respectively a straight up, a flat and a tapered structure as interconnect.

an optimal capacitive neutralization effect, the value of $C_N$ should correspond to $C_{gd}$ of the transistor, in this case 6 fF.

### C. Impedance Matching

Impedance matching is essential for high power gain. The maximum gain is only obtained when a conjugate match is applied at the input and the output of every stage. Differential slow-wave transmission lines [2] and on-chip transformers [3] are excellent building blocks for designing the matching networks. Slow-wave transmission lines are used to make a compact design. Floating dielectric strips in metal 8, beneath the differential lines (metal 9 and 10), reduce the wave speed as if the permittivity is increased. As a result, the physical transmission line length is reduced by a factor of 2.

In addition to transmission lines, on-chip transformers allow to decouple the different amplifier stages in common mode, which easily allows DC biasing. Moreover, in differential mode, it can be seen as an impedance transformer, and is thus suitable for matching networks. In this work, the four transformers have an inner diameter of 24 µm and a trace width of 10 µm. ADS Momentum simulations show that the transformer losses are below 0.6 dB at 160 GHz. The primary and secondary windings are designed in respectively metal 9 and 10, the two top-metal layers. They have a lower resistive loss due to the increased thickness. Another advantage of a transformer is the single-ended-to-differential conversion ability. Single-ended GSG probes are used for the measurements, so the transformers can act as a balun.

### D. Common-Mode Stability

As mentioned before, stability requires particular attention in mm-wave amplifiers [4]. If we consider the neutralized differential pair in common mode, a series resonant LC-tank is formed by the transformer's inductance and $C_N$ in parallel with $C_{gd}$. As a consequence, this can cause undesirable on-chip oscillations at lower frequencies, in the order of a few tens of GHz. To avoid this, a 1-kΩ resistor is

added to the bias network of every stage as shown in Fig. 1. The newly formed RLC-circuit forces a damped oscillation, which ensures a stable operation in common mode.

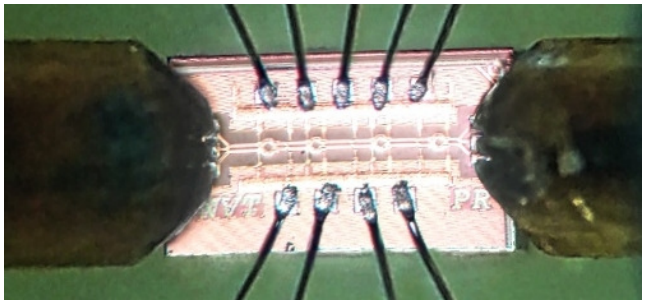


Fig. 4. Micrograph of aluminum bonded chip during measurements while GSG Picoprobes are landed.

## III. Amplifier Measurement Results

The three-stage amplifier is implemented in a TSMC 40-nm CMOS technology with 10 metal layers. The S-parameter measurements are performed using a Rohde & Schwarz ZVA40 Vector Network Analyzer with ZVA-220 extenders and a high performance Model 220 GSG Picoprobe with a pitch of 50 µm. The micrograph of the probed chip is depicted in Fig. 4. The measurement setup is calibrated using the LRRM calibration method and verified by Cascade Wincal XE software to ensure highly accurate results. The 160-GHz carrier is generated by a VDI WR5.1 AMC module. To measure the output power, an Erickson Instruments PM4 power meter is used.

Fig. 5 shows the chip micrograph. The entire chip measures 800x360 µm$^2$, including bond pads, GSG probe pads, ESD-diodes and decouple capacitors. The amplifier core itself covers an area of only 630x100 µm$^2$.

The amplifier is unconditionally stable if the Rollett's condition is satisfied, or $K>1$ and $\Delta<1$. As shown in Fig. 6, the amplifier is stable in the entire frequency band. The $\mu>1$ criterion for unconditional stability is also satisfied. Larger values of µ imply greater stability.

The outcome of the S-parameter measurements is presented in Fig. 7. It is clear from the figure that there is a good correspondence between simulation and measurement results. The measured power gain $s_{21}$ has a maximum value

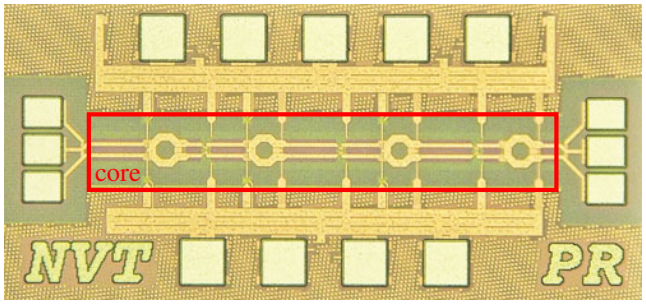



Fig. 5. Chip (0.8x0.36 mm$^2$) micrograph. Amplifier core region (0.63x0.1 mm$^2$) is marked by a red rectangle.

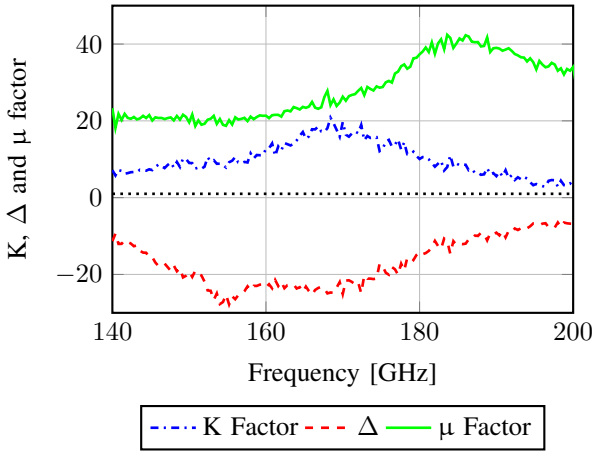



Fig. 6. Measured stability factor for K, Δ and µ test.

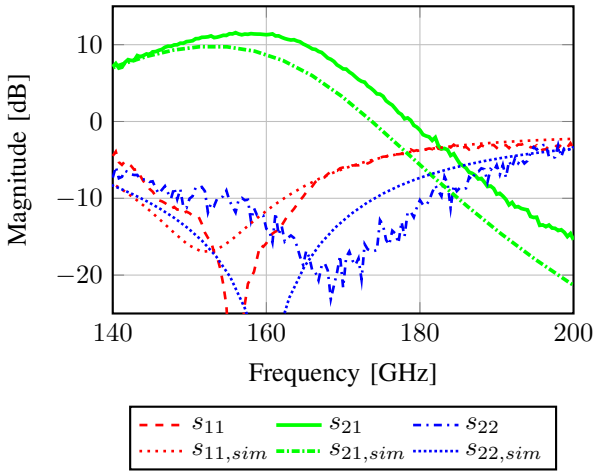



Fig. 7. Measured and simulated S-parameters vs. frequency. $s_{12}$ is below -40 dB, and therefore not represented.

of 11.6 dB around the center frequency of 160 GHz with a 3-dB bandwidth of 24 GHz. The large-signal measurement results are reported in Fig. 8 and Fig. 9. The measured 1-dB compression power at 160 GHz is 1.5 dBm and the maximum output power $P_{SAT}$ is 4.1 dBm. $P_{1dB}$, $P_{SAT}$ and the peak PAE are measured across the 24-GHz bandwidth as shown in Fig. 9. The DC power consumption is 42 mW with a supply voltage of 1.0 V and a bias voltage of 0.7 V.

Table I summarizes the performance of the proposed amplifier and gives a comparison to some previously published amplifiers. It can be seen that the amplifier achieves excellent results, despite the differential architecture and the high operating frequency. The high bandwidth is a notable factor and the measured group delay varies 10 ps within the 3-dB bandwidth, which makes the entire region suitable for operation.

## IV. Conclusion

A 160-GHz three-stage transformer-coupled fully-differential power amplifier with single-ended input and output was presented in this paper. To achieve this high frequency performance, a tapered gate-connection network

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUSLY PUBLISHED WORK.

| | RFIC '08 [5] | ISSCC '09 [6] | A-SSCC '10 [7] | APMC '13 [8] | **This Work** |
|---|---|---|---|---|---|
| Frequency [GHz] | 170 | 150 | 144 | 147 | **160** |
| Gain [dB] | 15 | 8.2 | 20.6 | 7.1 | **11.6** |
| Bandwidth [GHz] | 14 | 27 | 27 | N/A | **24** |
| No. of stages | 5 | 3 | 3 | 4 | **3** |
| Topology | Single Ended | Single Ended | Differential | Differential | **Differential** |
| $P_{1dB}$ [dBm] | 0 | 1.5 | 5 | N/A | **1.5** |
| $P_{SAT}$ [dBm] | >0 | 6.3 | 5.7 | N/A | **4.1** |
| $V_{DD}$ [V] | 3 | 1.1 | 2 | 2 | **1** |
| $P_{DC}$ [mW] | 135 | 25.5 | 102 | 104 | **42** |
| Core area [mm$^2$] | 0.044* | 0.16 | 0.05 | 0.19* | **0.063** |
| Technology | SiGe HBT | 65-nm CMOS | 65-nm CMOS | 65-nm CMOS | **40-nm CMOS** |

* Estimated from chip micrographs

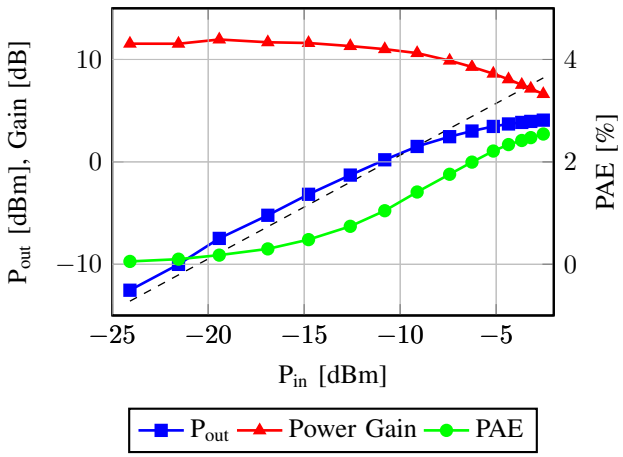



Fig. 8. Measured output power, power gain and PAE vs. input power at 160 GHz.

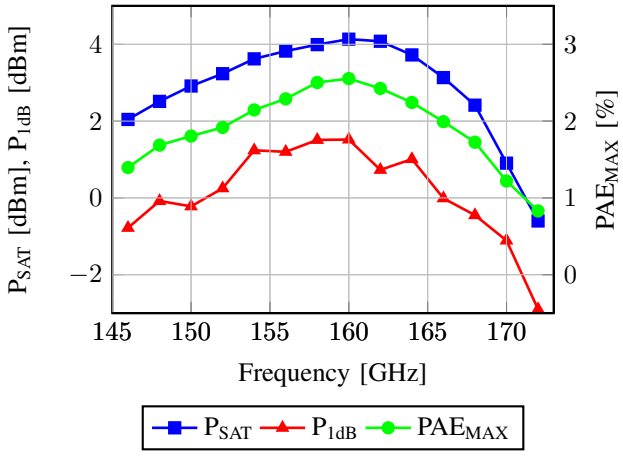



Fig. 9. Measured $P_{SAT}$, $P_{1dB}$ and $PAE_{MAX}$ vs. frequency.

was optimized. Slow-wave transmission lines and on-chip transformers act as matching networks. By making use of capacitive neutralization in the differential pairs and a series resistor in the bias lines, the amplifier remains stable in differential mode as well as common mode, resulting in a complete stability. The amplifier has an active area of 0.063 mm$^2$. The measurements yield a maximum gain of 11.6 dB. This could be achieved with only three stages, due to the combination of previously described techniques and the tapered gate-connection network.

## ACKNOWLEDGMENT

The authors would like to thank Frederik Daenen from KU Leuven ESAT/MICAS for measurement support.

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